Claims

- A leak current compensating device comprising:
 - a first power source terminal;
- a second power source terminal having a lower potential than said first power source terminal;

an output terminal;

a first transistor which is connected at one end to said first power source terminal and which has a conductive state, in which the first transistor outputs a predetermined voltage or current from the other end to said output terminal, and a cut-off state;

a second transistor of the same kind as said first transistor which is connected at one end to said first power source terminal and set in the cut-off state;

a third transistor which is interposed at a path for the flow of a leak current output from the other end of said second transistor to said second power source terminal, and a control terminal of which is connected to said path; and

a fourth transistor which constitutes a current mirror circuit with said third transistor and has a drive capacity to pass a current corresponding to the current flowing through said third transistor from

said output terminal to said second power source terminal.

2. A leak current compensating device in accordance with Claim 1, further comprising:

a fifth transistor which is interposed at a path for the flow of a leak current output from the other end of said second transistor to said second power source terminal, goes into the conductive state when said first transistor is in the cut-off state and goes into the cut-off state when the first transistor is in the conductive state; and

a sixth transistor which is interposed at a path from said output terminal to said second power source terminal through said fourth transistor, goes into the conductive state when said first transistor is in the cut-off state and goes into the cut-off state when the first transistor is in the conductive state.

- 3. A leak current compensating device in accordance with Claim 1, wherein the current drive capacity of said fourth transistor is equal or more than the leak current of said first transistor.
- 4. A leak current compensating device in accordance with Claim 1, wherein said first

transistor, said second transistor, said third transistor and said fourth transistor are MOS transistors or bipolar transistors.

5. A leak current compensating device in accordance with Claim 1, wherein

said first transistor is a PMOS transistor which is connected to said first power source terminal at source thereof and outputs a predetermined voltage or current from drain thereof to said output terminal;

an operational amplifier which has an inverting input terminal receiving a predetermined potential, a noninverting input terminal receiving an output voltage output from said output terminal directly or receiving a voltage generated by dividing said output voltage with resistance elements, and an output terminal outputting a control signal for controlling the gate of said first transistor, and brings said first transistor into the cut-off state in a predetermined case is further comprised;

said second transistor is a PMOS transistor which is connected to said first power source terminal at source and gate thereof and set in the cut-off state; and

said third transistor and said fourth

transistor are NMOS transistors which are connected to said second power source at each source, and said fourth transistor has a drive capacity to pass a current, which is predetermined times as large as the leak current of said second transistor, from said output terminal to said second power source terminal.

- 6. A leak current compensating method comprising:
- a first step of outputting a predetermined voltage or current from one end of said first transistor, the other end of which is connected said first power source terminal;

a second step of bringing said first transistor into the cut-off state;

a third step of inputting a leak current output from a second transistor of the same kind as said first transistor, which is connected at one end to said first power source terminal and set in the cut-off state, to one end and a control terminal of a third transistor, and passing the current from the other end of said third transistor to said second power source terminal having a lower potential than said first power source terminal; and

a fourth step of passing a current from one end of said first transistor to said second power source

terminal through said fourth transistor which constitutes a current mirror circuit with said third transistor and has a drive capacity to pass a current corresponding to the current flowing through said third transistor.

7. A leak current compensating method in accordance with Claim 6, wherein

in said second step, said fifth transistor which is interposed at a path for the flow of a leak current output from the other end of said second transistor to said second power source terminal and a sixth transistor which is interposed at a path from the other end of said first transistor to said second power source terminal through said fourth transistor are brought into the conductive state; and

in said first step, said fifth transistor and said sixth transistor are brought into the cut-off state.